UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,593	09/29/2003	Ichiro Yokokura	1614.1363	8553

21171 7590 10/31/2006

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,593	YOKOKURA ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-5 are objected to because of the following informalities:

a. In claim 1, line 15 "INC/DEC" is suggeseted to be changed to "increasing/decreasing (INC/DEC)".

b. In claim 2, page 26, lines 1-5, the phrase "has an up-down counter being counted up/down when a phase comparison signal, being an exclusive OR signal of said input clock and said output clock signal from said phase comparing part is HIGH/LOW, respectively" is suggested to be changed, for clarification, to the phrase "comprises an up-down counter being counted up/down when a phase comparison signal is HIGH/LOW, wherein the phase comparison signal is an exclusive OR signal of said input clock and said output clock signal from said phase comparing part, respectively;".

c. In claim 2, line 6, "DEC" is suggested to be changed to "decreasing (DEC)".

d. In claim 2, line 7, "INC" is suggested to be changed to "increasing (INC)".

e. In claim 3, line 21, "a computed phase difference" is suggested to be changed to "a computed phase difference;".

f. In claim 3, line 26, the word "described" is suggested to be changed to "stored".

g. In claim 4, lines 34-35, the phrase "each predetermined time interval" is suggested to be changed to "predetermined time intervals".

h. In claim 5, line 21, "an adoption rate" is suggested to be changed to "an execution rate" to conform with the terms used in the specification (see instant specification page 12, line 37-page 14, line 12.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 5 recite the limitation "A digital phase locked loop circuit for synchronizing a phase of an output clock signal with a phase of an input clock signal". However, claims 1 and 5 do not define when or how the clock signals are synchronized by the phase locked loop. Thus, claims 1-5 are deemed indefinite for not defining how or when the clock signals are synchronized.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U. S. Patent No. 5, 781, 054) in view of Garlepp et al. (U. S. Patent No. 6, 920, 622).

Regarding claim 5, Lee discloses a digital phase locked circuit (Fig. 1, column 1, lines 11-23)) for synchronizing a phase of an output clock signal represented by a phase locked clock signal with a phase of an input reference clock signal wherein the phase locked clock signal is generated by dividing a master clock signal as shown in Fig. 2 (see column 1, lines 23-32), comprising:

a phase comparing part (Fig. 1, block 100, column 1, lines 13-17) comparing the phase of the phase locked clock signal with the phase of the input reference clock signal; and

a phase comparison result detecting part (Fig. 2) referring to a phase lead/lag comparison result from the phase comparing part and outputting a signal from the mux (block 200) for increasing/decreasing a division rate for dividing the master clock signal (as described in column 1, lines 25-34) when the phase of the output clock signal leads or lags the phase of the input clock signal.

However, Lee does not disclose the phase locked loop comprises a control part changing phase absorption speed by controlling an execution (adoption) rate of the signal for increasing/decreasing the division number for dividing the master clock signal in accordance with a phase difference between the input clock signal and the master clock signal.

However, Garlepp et al. discloses a phase locked loop (see Fig. 7) which comprises of a control part including a phase compare logic (see Fig. 7, block 704) for comparing an output clock from a divider (Fig. 7, block 420) and an input clock (B). If the magnitude of the phase

difference between the clocks is greater than a certain value, the phase compare logic asserts a spit/swallow control signal to control the execution rate of the divider in order to provide an output clock signal one clock cycle early or one clock cycle late (see column 7, lines 47-59). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the phase locked loop of Lee to control the execution rate of the divider as disclosed by Garlepp et al. since Garlepp et al. states the phase adjustment provided by the control of the execution rate of the divider allows the operation of the phase detector well within its linear range (see column 8, lines 13-17).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Clark (U. S. Patent No. 4, 030, 045) and Kobayashi (US 2003/0076911) disclose controlling a rate of a divider is a phase locked loop.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
October 29, 2006